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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/938,106	08/23/2001	James M. Derderian	4832US (01-0104)	1038

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EXAMINER	
IM, JUNGHWA M	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/938,106	DERDERIAN, JAMES M.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-27,29-35,40-51 and 53-64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-27,29-35,40-51 and 53-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 23, 24, 29, 30, 33, 40, 45, 46, 49, 50, 53, 59 and 61-64 are rejected under 35 U.S.C. 102(e) as being anticipated by Wu et al. (US 6400007), hereafter Wu.

Regarding claims 23 and 45, Fig. 4 of Wu shows a device to use a method for assembling semiconductor devices with a densely stacked arrangement (col.2, line 64 through col. 3, line 61), comprising;

a first semiconductor device 28;

discrete conductive elements 32 over portions of said first semiconductor device and;

positioning a second semiconductor device 34 over the first semiconductor device, a back side of the second semiconductor device resting upon at least some of discrete conductive elements and being supported by being electrically isolated from each other (col.3, lines 54-56).

Regarding the limitation of "a back side of the second semiconductor device ... being supported thereby, " Fig. 5 of Wu shows that the discrete conductive elements (the wires) contributes to support the back side of the second semiconductor device with adhesive layers (50, 52) since the wires are in the direct contact beneath the back side of the second

semiconductor device. In addition, Examiner would like to point out that the second (upper) semiconductor device is supported *collectively* by other elements under the second semiconductor device such as the wires and the adhesive layer through forming a complete package. Note that even the lower (first) semiconductor contributes a part of the collective support for the upper semiconductor device. That is, all elements connected directly or indirectly to one another is "collectively support one another."

Regarding the limitation in the preamble of claim 45, Fig. 4 of Wu shows "semiconductor device in a stacked arrangement with stacked arrangement having a height substantially equal to combined thickness of each of the semiconductor device and distances discrete conductive elements associated therewith protrude above said each of the semiconductor devices." In addition, note that the limitation in the preamble does not have patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *Kropa v. Robie*, 88 USPQ 478 (CCPA 1951).

Regarding claims 24 and 46, Wu discloses positioning the second semiconductor device comprises positioning the second semiconductor device on said at least some of discrete conductive elements with the back side and the discrete conductive elements in mutual electrical isolation (col.3, lines 54-56).

Regarding claims 29 and 49, Wu discloses a quantity of adhesive material 50 to at least an active surface of the first semiconductor device (col.3, lines 24-25).

Regarding claims 30 and 50, it is inherent that the device of Wu shows drawing the second semiconductor device toward the first semiconductor device after applying the adhesive on the first device since the adhesive is applied on the active surface of the first semiconductor device and positioning the second semiconductor device is followed.

Regarding claims 33 and 53, it is inherent that the applying is effected after the positioning the second semiconductor device since positioning the second semiconductor device has to be done before permanent adhering to the first semiconductor device.

Regarding claims 40 and 59, Wu discloses securing the first semiconductor device and a substrate to one another (col.3, lines 16-20).

Regarding claim 61, it is inherent that electrical communication would be established between bond pads of the second semiconductor device (34) and the corresponding contact areas of the substrate (col. 3, lines 41-43) in order to have the device operate functionally.

Regarding claim 62, Fig. 4 of Wu shows establishing communication comprises placing additional discrete conductive elements (56; wires) between each of the bond pads and the corresponding contact area of the corresponding contact areas.

Regarding claim 63, Fig. 4 of Wu shows proving at least one connective elements (42; signal output terminal) in communication with at least one bond pad of each of said first and second semiconductor devices (col. 3, lines 4-8).

Regarding claim 64, Wu discloses a method further comprising encapsulating (58 in Fig. 4; a packaging layer) said first and second semiconductor devices (col. 3, lines 44-47).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 25, 26, 31, 34, 35, 41-44, 47, 51, 54-58 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable under obviousness over Wu in view of Lee et al. (US 6,388,313), hereafter Lee.

Regarding claims 25 and 47, Wu discloses the most aspect of the instant invention except "providing a dielectric coating on at least portion of said discrete conductive elements." Lee discloses a method providing a dielectric coating on at least portion of said discrete conductive elements (col. 5, lines 40-44). It would have been obvious to one of ordinary skill in the art at the time of the invention to apply a coat on the discrete conductive elements (wires) of Wu's device with the teaching of Lee in order to prevent a short circuit between the semiconductor device and the bare wires.

Regarding claim 26, Lee shows a method wherein the providing comprises forming at least one of a dielectric oxide and a dielectric polymer coating on at least said portions of the discrete conductive elements (col. 5, lines 22-24).

Regarding claims 31 and 51, Wu does not disclose "said drawing is effected by at least one of capillary action of the adhesive material, curing of the adhesive material, application of heat to the adhesive material, and vibration of the adhesive material." However, it would be obvious that such drawing is effected by one of the effects recited by the pending claim since

Wu's adhesive material (resin) is identical to the one recited in the instant invention. Furthermore, Lee discloses the drawing is effected by at least curing of the adhesive material (resin) and application of heat to the adhesive material (curing; col. 5, lines 32-40).

The limitations regarding claims 34 and 35 have been discussed in claims 30 and 31 with the combined teaching of Wu and Lee.

Regarding claim 41, Wu does not disclose " said placing the discrete conductive elements comprises securing the discrete conductive elements to contact areas of the substrate and the bond pads of the first semiconductor device." Lee shows a method wherein the placing the discrete conductive elements comprises securing the discrete conductive elements to contact areas of the substrate and the bond pads of the first semiconductor device (col. 5, lines 8-10). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Lee into the device of Wu in order to have signals transferred between the stacked devices through having the discrete conductive elements (wires) secured on the contact areas (bond pads) on the substrate.

Regarding claim 42, Lee shows the securing comprises electrically connecting bond pads of the second semiconductor device to the corresponding contacts areas of the substrate (col. 5, lines 13-16).

Regarding claim 43, Lee shows encapsulating at least portion of at least one of the substrate, the first semiconductor device, and the second semiconductor device (col. 6, lines 32-36).

Regarding claim 44, Lee shows forming external conductive elements 27 in Fig. 1 on the substrate in electrical communication with corresponding contact areas (col. 5, lines 1-4).

Limitations of claims 54 and 55 have been discussed in claims 34 and 35.

Regarding claim 56, Wu fails to disclose "biasing at least one of the first and second semiconductor devices toward the other of the first and second semiconductor devices." Lee shows biasing at least one of the first and second semiconductor devices toward the other of the first and second semiconductor devices (col. 4, lines 54-68). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Lee into the device of Wu in order to have an electrical connection for a necessary circuit configuration of the device.

Regarding claim 57, Lee shows controlling the biasing by means of adhesive (col. 4, lines 54-68).

Regarding claim 58, Lee shows the controlling the biasing comprises controlling the biasing force to a level sufficient to deform, kink, bend, or collapse the discrete conductive elements.

See the respective portions of the specification such as col. 5, lines 24-32.

Regarding claim 60, Wu fails to show "connecting the discrete conductive elements to corresponding contact areas of the substrate." Lee shows connecting the discrete conductive elements to corresponding contact areas of the substrate (col. 5, lines 8-10). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Lee into the device of Wu in order to have current flow from supply contact areas of the substrate to the semiconductor devices through the discrete conductive elements (wires).

Claims 27, 32 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable under obviousness over Wu in view of Shim et al. (US 6,531,784), hereafter Shim.

Regarding claims 27 and 48, Wu does not disclose positioning a dielectric layer at least portions of the backside of the second semiconductor device. Fig. 7 of Shim shows the dielectric layer (50C) on the portion of the backside of the second semiconductor device. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Shim into the device of Wu in order to enhance the electrical isolation between the devices and the wires.

Regarding claim 32, Wu does not disclose positioning a dielectric layer at least portions of the backside of the second semiconductor device. Fig. 3 of Shim shows the dielectric layer (44) on the portion of the backside of the second semiconductor device. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Shim into the device of Wu in order to mount two devices securely.

Response to Arguments

Applicant's arguments filed January 10, 2005 have been fully considered but they are not persuasive.

1. Applicant mainly argues that "Wu does clearly describe, however, that wires 32 may be 'pressed' by second semiconductor die 34 (col. 3, lines 54-56), indicating that wires 32 do not support second semiconductor die 34 but, rather, collapse under the small weight of second semiconductor device 34. Wu also clearly explains that the second semiconductor die 34 'is stacked above' the first semiconductor die 28 'by adhered glue 50,' indicating that adhered glue

50 supports second semiconductor die 34. Col. 3, lines 36-40." Such argument is not persuasive. It is pointed out that "resting upon" in general indicates a state of motionless or inactivity. And it is a nature of physics that an object being rested upon is indeed being pressured by an element on top of it. With this understanding, it is obvious that the wires 32 in Fig. 4 of Wu are in an inert state of being pressed, not in active mode of being pressed to result in a collapse of the wires leading to a collapse or malfunctioning of the entire device. Therefore, Fig. 4 of Wu shows "a back side of the second semiconductor device resting upon at least some of discrete conductive elements," and "on at least some of discrete conductive elements" since Fig. 4 of Wu shows second semiconductor die 34 contacting wires 32. It is also pointed out that the elected embodiment in Fig. 12-17 of the insant invention does not disclose that discrete conductive elements alone support the second semiconductor device. The instant invention clearly shows that substantially the entire back surface of the second semiconductor device, that is, the second semiconductor device is supported mainly by the adhesive also.

2. Applicant further argues that "Moreover, without wires 32, adhered glue 50 and element 54 would, either alone or together, support second semiconductor die 34. Therefore, wires 32 are not needed to support second semiconductor die 34. Thus, Wu lacks any inherent description that wires 32 support the second semiconductor die 34." It is pointed out that the instant claim does not recite that discrete conductive elements are the only elements supporting the second semiconductor device. Again, the instant invention also shows that substantially the entire back surface of the second semiconductor device, that is, most portion of the second semiconductor device is supported mainly by the adhesive also.

3. Applicant argues that "Wu lacks any express or inherent description of positioning a second semiconductor die 34 over wires 32 with a back side of the semiconductor die 34 and wires 32 'in mutual electrical isolation.' "Wu explicitly discloses that the wires 32 and the second semiconductor device are free from being short circuited, in other words, "in mutual electrical isolation."

4. Applicant argues that "Wu does not expressly or inherently describe 'drawing' second semiconductor die 34 thereof toward first semiconductor die 28." As discussed in the office action, it is noted that drawing is an intrinsic reaction when the adhesive is applied between the first semiconductor die and the second semiconductor die. Furthermore, the second semiconductor die has to be drawn toward the first semiconductor die since first semiconductor die is already secured on the substrate. Examiner also pointed out that Lee details this specific reaction.

5. Applicant argues that Wu includes no express or inherent description that a quantity of adhesive material (adhered glue 50 or element 54) is applied to an active surface of first semiconductor die 28 'after. . . positioning the second semiconductor' die 34 thereover." It is pointed out that it is obvious that applying is *effected* after positioning the second semiconductor since the second semiconductor die has to be positioned before applying adhesive, and after then applying the adhesive is effected to glue the second semiconductor die to the first semiconductor die.

6. Finally, Applicant argues that Wu and Lee do not teach specific/recited reactions such as drawing between two semiconductor devices when the adhesive is applied. As discussed in

the Office Action, Lee details those specific reactions. In addition, those reactions are intrinsic when the adhesive is applied between two semiconductor devices.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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